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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/639,432	08/14/2000	Vladimir Kljajic	TI-29645	1222

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J Dennis Moore
Texas Instruments Incorporated
P O Box 655272 M/S 3999
Dallas, TX 75265

EXAMINER	
MUNOZ, GUILLERMO	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 09/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/639,432	KLJAJIC ET AL.	
	Examiner	Art Unit	
	Guillermo Munoz	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4,5,10,11,14,15 and 17-19* is/are allowed.

6)☒ Claim(s) *1-3,6-9,12,13,16, and 20-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/13/2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed June 24, 2004 have been fully considered but they are not persuasive.

Applicant argues Loyer does not disclose or suggest the following limitations: a composite divisor to produce a quotient and remainder, a first divisor component corresponding to the quotient, or a second divisor component corresponding to the remainder.

Examiner response—

As applied to Applicants argument that Loyer fails to teach a quotient and remainder, the claimed limitations are inherently produced by Loyer's division process.

As applied to Applicants argument that Loyer fails to teach a quotient corresponding to the first divisor component and remainder corresponding to second divisor component. Examiner understands instant application as follows:

The divisor generator produces a quotient and remainder by division of the base clock by the product of the desired baud rate and the oversampling factor as is done in conventional interface units, note instant application page 6, lines 16-17. Claim 1 recites "dividing the base clock signal in response to said composite divisor to produce a quotient and remainder *and* produce a baud clock signal". It is clear from figures 1 and 2 that the divisor generator produces the quotient and remainder, therefore, the composite divisor is interpreted to be the desired baud rate and oversampling factor divisors as found in conventional interface units. The quotient and remainder are provided to the clock divider element 13 of figure 1.

It is not clear from the specification or the figures how the first component (i.e. the desired baud clock) of the divisor generator corresponds to the quotient or how the second component (oversampling factor) of the divisor generator corresponds to the remainder.

Furthermore, the phrase "and produce" in the claim 1 quotation above, is interpreted to indicate that the base clock is divided by the composite divisor to produce a baud clock signal.

From the above understanding of composite divisor, division of the base clock by the composite divisor to produce a baud clock signal is not enabled by the instant application. Therefore, the language of claim 1 should be re-worded to more accurately describe the disclosed invention.

Withdraw of Indication of Allowable Subject Matter

The indicated allowability of claims 6-9 is withdrawn in view of the newly cited reasoning(s) to Loyer et al.. Rejections based on the newly cited reasoning(s) follow.

Drawings

The drawings are objected to under 37 CFR 1.83(a) because they fail to show the base clock and the oversampling factor being provided to the Divisor Generator element 11 of figure 1 as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one

figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-3, 7, 12, 13, and 20-30 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for base clock divided by a quotient and remainder , which are generated from a division of the base clock by the product of a desired baud rate and an oversampling factor, does not reasonably provide enablement for a base clock divided by a composite divisor to produce a baud clock. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims.

Regarding claim 1; the divisor generator produces a quotient and remainder by division of the base clock by the product of the desired baud rate and the oversampling factor as is done in conventional interface units, note instant application page 6, lines 16-17. Claim 1 recites "dividing the base clock signal in response to said composite divisor to produce a quotient and remainder *and* produce a baud clock signal" it is clear from figures 1 and 2 that the divisor generator produces the quotient and remainder, thus the composite divisor is interpreted to be the combination of the desired baud rate and oversampling factor. The quotient and remainder are provided to the clock divider element 13 of figure 1. It is not clear from the specification or the figures how the first component (desired baud clock) of the divisor generator corresponds to the quotient or how the second component (oversampling factor) of the divisor generator corresponds to the remainder.

Claims 2-3 are dependent on rejected claim 1 and are rejected under 35 U.S.C. 112, first paragraph.

Regarding claim 7, see claim 1.

Regarding claim 12; as applied to claim 1, the phrase "which is indicative of a minimum time interval based on a first divisor component corresponding to said quotient...an extended time interval based to a second divisor component corresponding to said remainder" render the claim un-enabling for the reasoning applied to claim 1.

Claims 13 and 20 are dependent on rejected claim 12 and are rejected under 35 U.S.C. 112, first paragraph.

Regarding claim 21, see claim 12.

Claims 22-23 are dependent on rejected claim 21 and are rejected under 35 U.S.C. 112, first paragraph.

Regarding claim 24, see claim 12.

Claims 25-27 are dependent on rejected claim 24 and are rejected under 35 U.S.C. 112, first paragraph.

Regarding claim 28, see claim 12.

Claim 29 is dependent on rejected claim 28 and is rejected under 35 U.S.C. 112, first paragraph.

Regarding claim 30, see claim 12.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 8, 9, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loyer et al..

Regarding claim 6; as applied to the examiners interpretation to the composite divisor as explained above in Examiners response, Loyer et al. disclose Autobauding With Adjustment To A Programmable Baud Rate which teaches all the claimed subject matter "selecting a desired baud rate...second divisor component" in claim 6 as follows: selecting a desired baud rate is anticipated by step 504 and 506 of figure 6; providing a composite divisor is anticipated by elements 302 and 304 of figure 3; the minimum time interval is anticipated by the resulting

interval based on the baud divider divisor; at least one pair of adjacent pulses is anticipated by the resulting time interval that results from the base clock divided by the desired baud divisor and the oversampling divisor, using this interpretation at least one pair includes all pairs of adjacent leading edges; baud clock signal has a baud rate that approximates the desired baud rate is anticipated by baud clock output 203 of figure 3, however, Loyer et al. do not explicitly state providing a programmable oversampling factor, which is interpreted to be the second component of the composite divisor.

It would have been within the level of one having ordinary skill in the art at the time of the invention to provide a programmable oversampling factor, since Loyer et al.'s teaching of oversampling by a particular factor in Col.6, lines 10-12, suggest various oversampling factors may be implemented.

Regarding claim 8; as applied to claim 6, Loyer et al. further teach the claimed subject matter "more closely approximates the desired baud rate" by the functionality of the BAUD DIVISOR_THRESHOLD value, note Col.7 line 65 – Col.8, line 13.

Regarding claim 9; as applied to claim 16, Loyer et al. do not explicitly teach the claimed subject mater "indexing", however, the operation of addressing the plurality of registers is the same.

Regarding claim 16; as applied to claim 6 above, although Loyer et al. do not specifically disclose that the divisor generator includes a look-up table having information stored that associates with baud rates and divisor components. Loyer et al. teach that divisor values and an associated threshold value associated with a particular baud rate is stored in a plurality of storage registers. The limitations in claim 16 do not define a patentable distinct invention over that in

Loyer et al. since both the invention as a whole and Loyer et al. are directed to storing information associated with a baud rates and divisor components. The implementation of the storage element in which the information is held presents no new or unexpected results, so long as the information is retrievable as required. If one has more baud rates than available storage registers, more efficient storage would be required. Therefore, to have one look-up table that stores the information associated with a plurality of baud rates would have been routine experimentation and optimization in the absence of criticality.

Allowable Subject Matter

Claims 4-5, 10-11, 14-15, and 17-19 are allowed.

The following is an examiner's statement of reasons for allowance:

Claims 4-5, 10-11, and 14-19 are allowed because the claimed invention comprises a baud clock generator, which generates a baud clock signal having leading edges of adjacent pulses with the baud period that vary by a minimum interval or a extended interval based on a quotient and remainder, respectively. A conventional baud clock generator circuit generates the quotient and remainder. The closest prior art, Loyer et al. (cited in office action mailed March 25, 2004) teach a conventional baud clock generator circuit including a composite divisor, which comprises the desired baud rate divisor and the oversampling divisor, however Loyer et al. fail to teach using the quotient for generating the minimum and extended time intervals and the remainder for selecting the adjacent leading edges separated by the extended time interval. These distinct features have been included in independent claims 4, 10, 14, and 17, rendering them allowable. Claims 5, 11, 15, and 18-19 are depend on independent claims 4, 10, 14, and 17, respectively, and are thereby allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guillermo Munoz whose telephone number is 571-272-3045. The examiner can normally be reached on Monday-Friday 8:30a.m-4:30p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GM
September 8, 2004

JEAN B. CORRIELUS
PRIMARY EXAMINER
9/16/04